winbond

8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION 2
2. FEATURES 2
3. PIN CONFIGURATIONS 3
4. PIN DESCRIPTION 4
5. FUNCTIONAL DESCRIPTION 5
   5.1 Eight-source interrupt informations: 6
6. ON-CHIP FLASH EPROM CHARACTERISTICS 10
7. SECURITY BITS 12
8. ABSOLUTE MAXIMUM RATINGS 13
9. DC CHARACTERISTICS 14
10. AC CHARACTERISTICS 16
11. TIMING WAVEFORMS 19
12. TYPICAL APPLICATION CIRCUITS 22
13. PACKAGE DIMENSIONS 24

1. GENERAL DESCRIPTION

The W78L054A is an 8-bit microcontroller which can accommodate a wide supply voltage range with low power consumption. The instruction set for the W78L054A is fully compatible with the standard 8051. The W78L054A contains an 16K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L054A allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

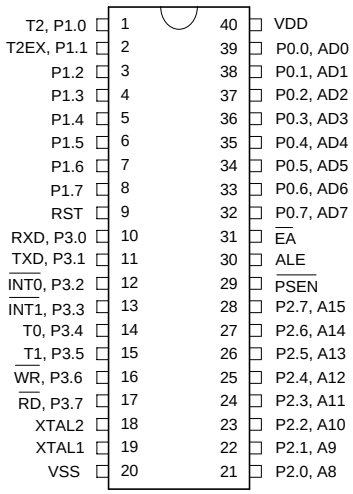
The W78L054A microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

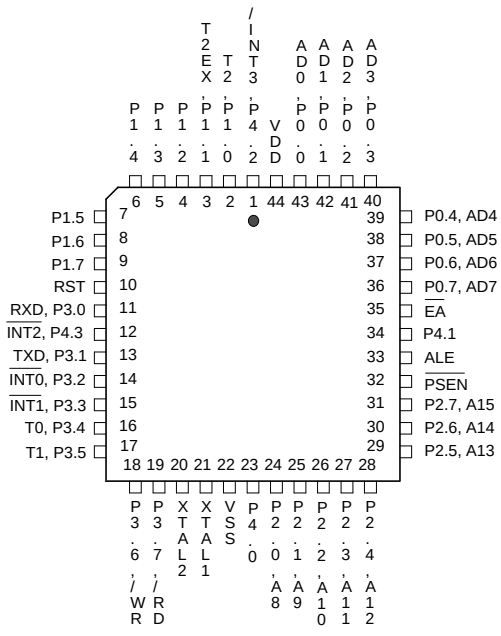
- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 16 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional $\overline{\text{INT2}}$ / $\overline{\text{INT3}}$ *(available on 44-pin PLCC/QFP package)*
- Three 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Eight sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - Lead Free (RoHS) DIP 40: W78L054A24DL
  - Lead Free (RoHS) PLCC 44: W78L054A24PL
  - Lead Free (RoHS) PQFP 44: W78L054A24FL

3. PIN CONFIGURATIONS

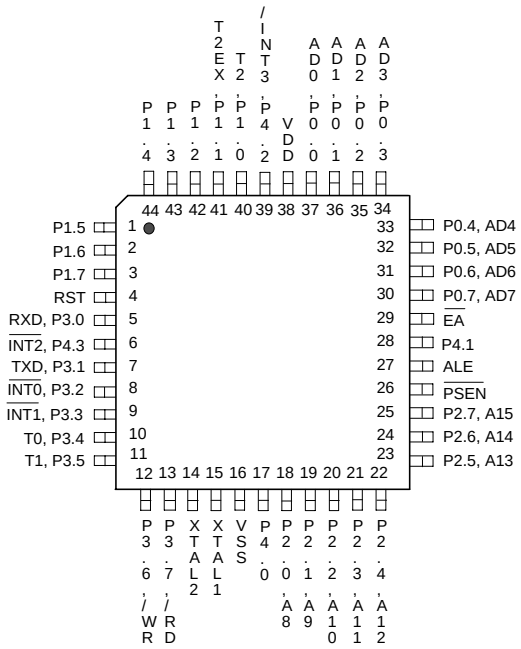
40-Pin DIP



44-Pin PLCC



44-Pin QFP



4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
$\overline{EA}$	**EXTERNAL ACCESS ENABLE**: This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be presented on the bus if $\overline{EA}$ pin is high and the program counter is within on-chip ROM area.
$\overline{PSEN}$	**PROGRAM STORE ENABLE**: $\overline{PSEN}$ enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs from this pin.
ALE	**ADDRESS LATCH ENABLE**: ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	**RESET**: A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1.
V_{SS}	**GROUND**: Ground potential
V_{DD}	**POWER SUPPLY**: Supply voltage for operation.
P0.0–P0.7	**PORT 0**: Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The Port 0 is also an open-drain port and external pull-ups need to be connected while in programming.
P1.0–P1.7	**PORT 1**: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control
P2.0–P2.7	**PORT 2**: Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	**PORT 3**: Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port receiver input TXD(P3.1) : Serial Port transmitter output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$(P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) :External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	**PORT 4:** Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

5. FUNCTIONAL DESCRIPTION

The W78L054A architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78L054A: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt $\overline{INT2}$, $\overline{INT3}$ has been added to either the PLCC or QFP 44 pin package. And description follows:

1. $\overline{INT2}$ / $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

XICON - external interrupt control (C0H)

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

5.1 Eight-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

Example:

```
P4      REG   0D8H
MOV     P4, #0AH      ; Output data "A" through P4.0–P4.3.
MOV     A, P4         ; Read P4 status to Accumulator.
ORL     P4.#00000001B
ANL     P4.#11111110B
```

3. Reduce EMI Emission

Because of on-chip Flash EPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space. The AO bit in the AUXR register, when set, disables the ALE output. In order to reduce EMI emission from oscillation circuitry, W78L054A allows user to diminish the gain of on-chip oscillator amplifiers by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

*****AUXR - Auxiliary register (8EH)**

-	-	-	-	-	-	-	AO

AO: Turn off ALE output.

4. Power-off Flag

*****PCON - Power control (87H)**

-	**-**	-	**POF**	GF1	GF0	PD	IDL

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when V_{DD} has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

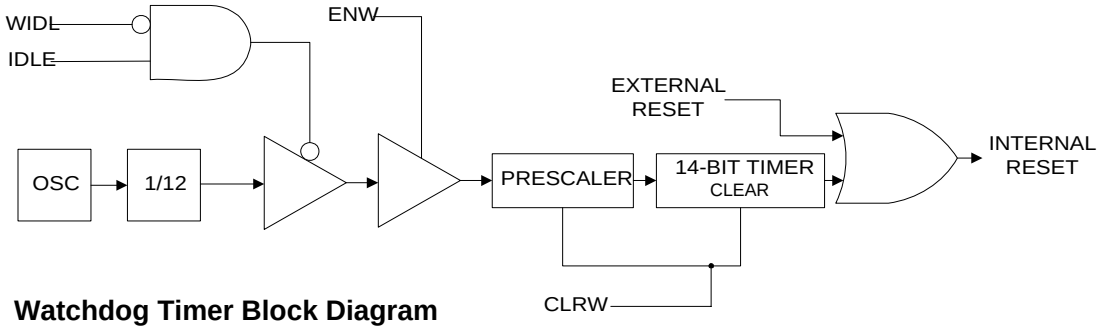
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2~0 as follows:

PS2	PS1	PS0	PRESCALER SELECT
0	0	0	2
0	1	0	4
0	0	1	8
0	1	1	16
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

The time-out period is obtained using the following equation:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	WATCHDOG TIME-OUT PERIOD
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 ms
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

Clock

The W78L054A is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L054A relatively insensitive to duty cycle variations in the clock. The W78L054A incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L054A is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

6. ON-CHIP FLASH EPROM CHARACTERISTICS

The W78L054A has several modes to program the on-chip Flash EPROM. All these operations are configured by the pins RST, ALE, $\overline{PSEN}$, A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3), $\overline{CE}$ (P3.6), $\overline{OE}$ (P3.7), A0(P1.0) and V_{PP}($\overline{EA}$). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

Output Disable Condition

When the $\overline{OE}$ is set to high, no data output appears on the D7..D0.

Program Operation

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the Vpp is reach to Vcp (12.5V) level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

Erase Operation

An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the Vpp is reach to Vep level, $\overline{CE}$ set to low, and $\overline{OE}$ set to high.

Erase Verify Operation

After an erase operation, all of the bytes in the chip must be verified to check whether they have been successfully erased to 1 or not. The erase verify operation automatically ensures a substantial erase margin. This operation will be done after the erase operation if Vpp = Vep(14.5V), $\overline{CE}$ is high and $\overline{OE}$ is low.

Program/Erase Inhibit Operation

This operation allows parallel erasing or programming of multiple chips with different data. When P3.6($\overline{CE}$) = V_{IH}, P3.7($\overline{OE}$) = V_{IH}, erasing or programming of non-targeted chips is inhibited. So, except for the P3.6 and P3.7 pins, the individual chips may have common inputs.

OPERATIONS	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ($\overline{CE}$)	P3.7 ($\overline{OE}$)	$\overline{EA}$ (V_{PP})	P2, P1 (A15..A0)	P0 (D7..D0)	NOTE
Read	0	0	0	0	0	0	1	Address	Data Out	
Output Disable	0	0	0	0	0	1	1	X	Hi-Z	
Program	0	0	0	0	0	1	V_{CP}	Address	Data In	
Program Verify	0	0	0	0	1	0	V_{CP}	Address	Data Out	@3
Erase	1	0	0	0	0	1	V_{EP}	A0:0, others: X	Data In 0FFH	@4
Erase Verify	1	0	0	0	1	0	V_{EP}	Address	Data Out	@5
Program/Erase Inhibit	X	0	0	0	1	1	V_{CP}/ V_{EP}	X	X	

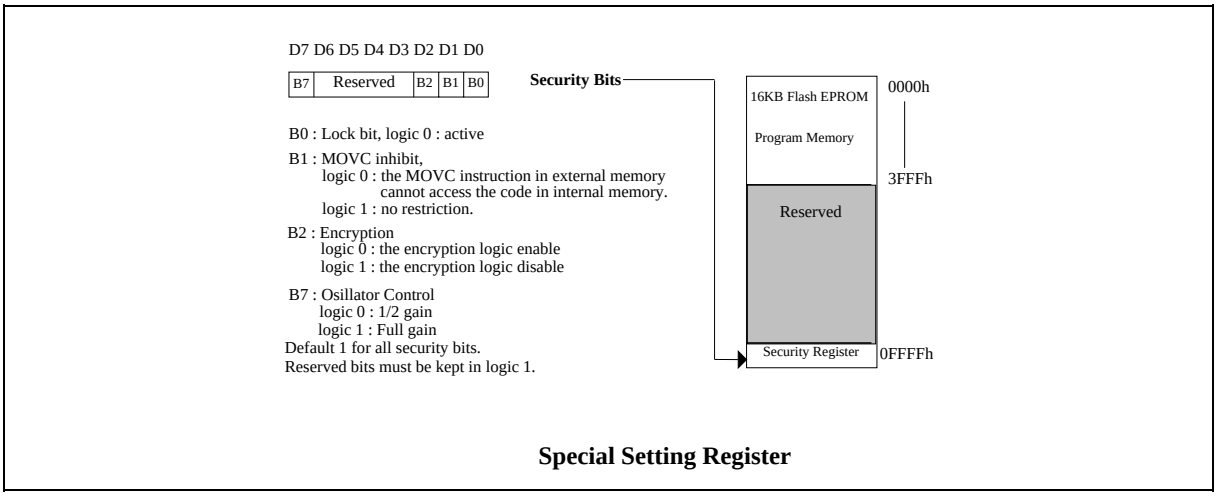
Notes:

1. All these operations happen in RST = V_{IH}, ALE = V_{IL} and $\overline{PSEN}$ = V_{IH}.
2. V_{CP} = 12.5V, V_{EP} = 14.5V, V_{IH} = V_{DD}, V_{IL} = Vss.
3. The program verify operation follows behind the program operation.
4. This erase operation will erase all the on-chip Flash EPROM cells and the Security bits.
5. The erase verify operation follows behind the erase operation.

7. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78L054A has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The Security register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



Special Setting Register

Lock bit

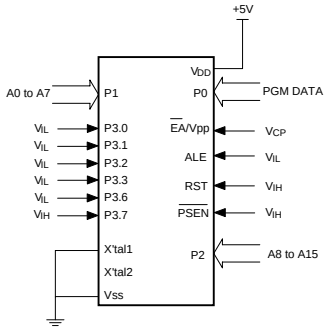
This bit is used to protect the customer's program code in the W78L054A. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

MOVC Inhibit

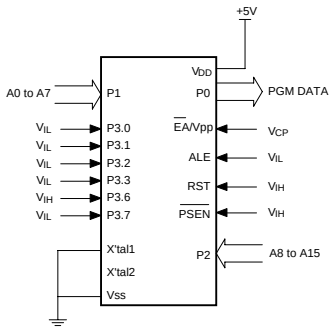
This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



Programming Configuration



Programming Verification

8. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD}-V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9. DC CHARACTERISTICS

V_{SS} = 0V, T_A = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	2.4	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
		-	3	mA	No load V_{DD} = 2.4V
Idle Current	I_{IDLE}	-	6	mA	V_{DD} = 5.5V, Fosc =20 MHz
		-	1.5	mA	V_{DD} = 2.4V, Fosc =12 MHz
Power Down Current	I_{PWDN}	-	50	µA	V_{DD} = 5.5V, Fosc =20 MHz
		-	20	µA	V_{DD} = 2.4V, Fosc =12 MHz
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
		0	0.5	V	V_{DD} = 2.4V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
		0	0.3	V	V_{DD} = 2.4V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Input High Voltage	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
P0, P1, P2, P3, P4, $\overline{EA}$		1.4	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
RST[*1]		1.7	V_{DD} +0.2	V	V_{DD} = 2.4V
Input High Voltage	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
XTAL1 [*3]		1.6	V_{DD} +0.2	V	V_{DD} = 2.4V
Output Low Voltage	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
P1, P2, P3, P4		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +1 mA
Output Low Voltage	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
P0, ALE, $\overline{PSEN}$ [*2]		-	0.25	V	V_{DD} = 2.4V, I_{OL} = +2 mA
Sink Current	I_{SK1}	4	12	mA	V_{DD} = 4.5V, Vin = 0.45V
P1, P2, P3, P4		1.8	5.4	mA	V_{DD} = 2.4V, Vin = 0.45V
Sink Current	I_{SK2}	8	16	mA	V_{DD} = 4.5V, Vin = 0.45V
P0, ALE, $\overline{PSEN}$		4.5	9	mA	V_{DD} = 2.4V, Vin = 0.4V
Output High Voltage	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -100 μA
P1, P2, P3, P4		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -8 μA
Output High Voltage	V_{OH2}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = -400 μA
P0, ALE, $\overline{PSEN}$ [*2]		1.4	-	V	V_{DD} = 2.4V, I_{OH} = -200 μA
Source Current	I_{SR1}	-100	-250	μA	V_{DD} = 4.5V, Vin = 2.4V
P1, P2, P3, P4		-20	-50	μA	V_{DD} = 2.4V, Vin = 1.4V
Source Current	I_{SR2}	-8	-14	mA	V_{DD} = 4.5V, Vin = 2.4V
P0, ALE, $\overline{PSEN}$		-1.9	-3.8	mA	V_{DD} = 2.4V, Vin = 1.4V

Notes:

*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

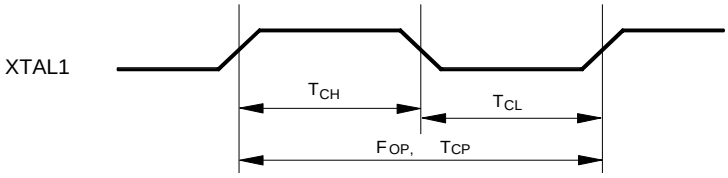
*3. XTAL1 is a CMOS input.

*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

10. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	20	MHz	1
Clock Period	T_{CP}	50	-	-	nS	2
Clock High	T_{CH}	25	-	-	nS	3
Clock Low	T_{CL}	25	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP} -Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP} -Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP} -Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP} -Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP} -Δ	3 T_{CP}	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP} -Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP} -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP} -Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP} -Δ	6 T_{CP}	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 T_{CP}	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 T_{CP}	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

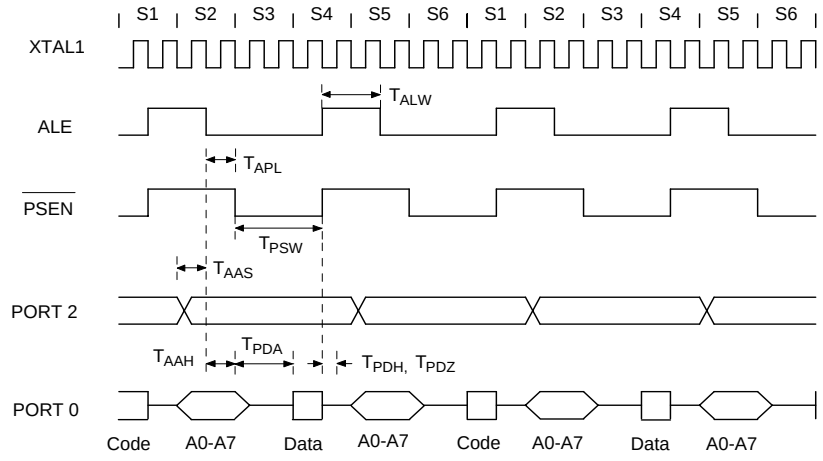
Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
V_{PP} Setup Time	T_{VPS}	2.0	-	-	µS
Data Setup Time	T_{DS}	2.0	-	-	µS
Data Hold Time	T_{DH}	2.0	-	-	µS
Address Setup Time	T_{AS}	2.0	-	-	µS
Address Hold Time	T_{AH}	0	-	-	µS
$\overline{CE}$ Program Pulse Width for Program Operation	T_{PWP}	290	300	310	µS
OECTRL Setup Time	T_{OCS}	2.0	-	-	µS
OECTRL Hold Time	T_{OCH}	2.0	-	-	µS
$\overline{OE}$ Setup Time	T_{OES}	2.0	-	-	µS
$\overline{OE}$ High to Output Float	T_{DFP}	0	-	130	nS
Data Valid from $\overline{OE}$	T_{OEV}	-	-	150	nS

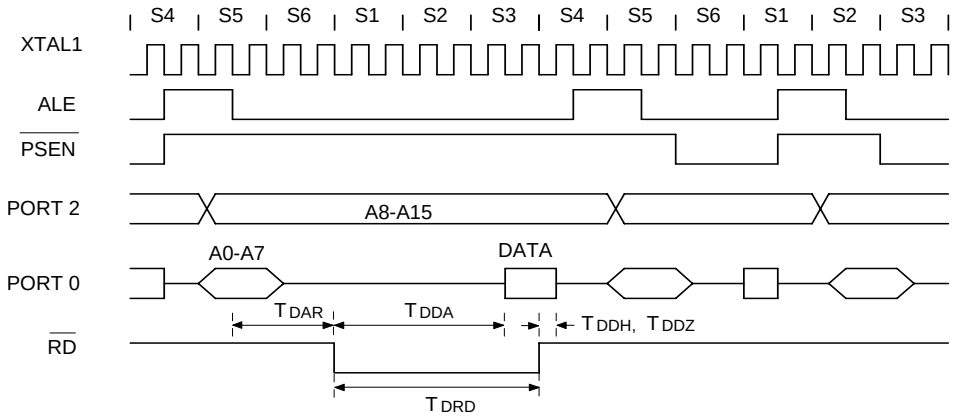
Note: Flash data can be accessed only in flash mode. The RST pin must pull in V_{IH} status, the ALE pin must pull in V_{IL} status, and the $\overline{PSEN}$ pin must pull in V_{IH} status.

11. TIMING WAVEFORMS

Program Fetch Cycle

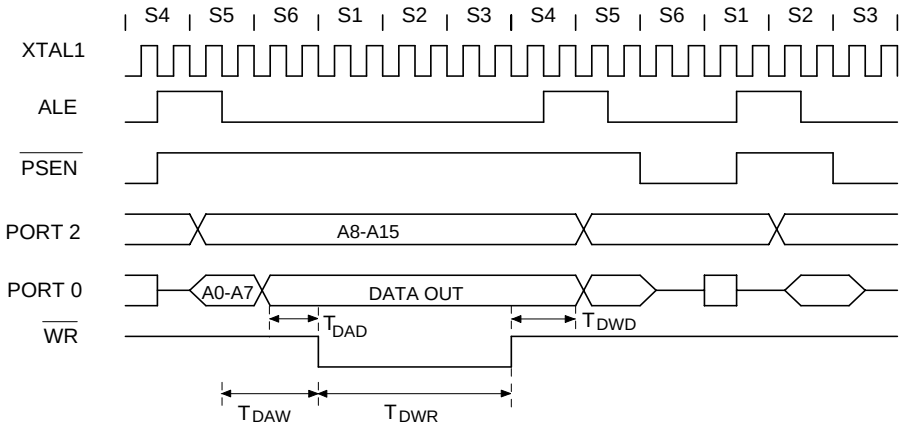


Data Read Cycle

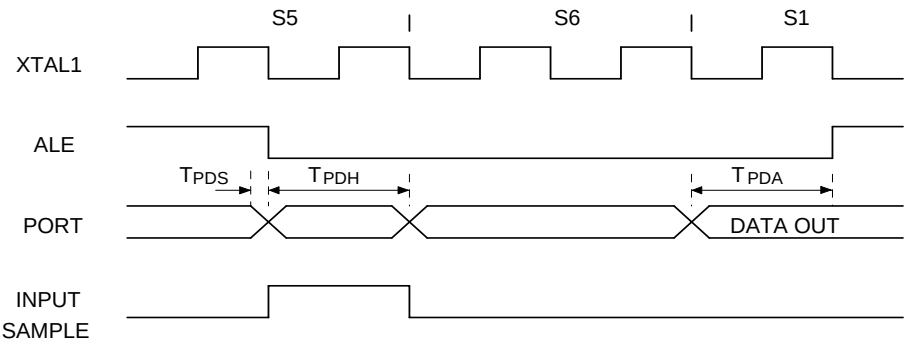


Timing Waveforms, continued

Data Write Cycle

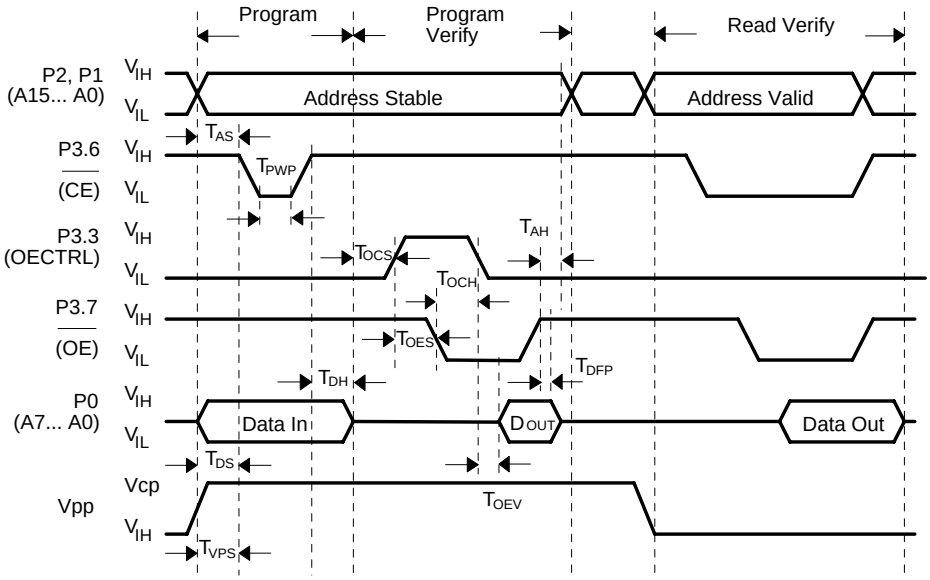


Port Access Cycle



Timing Waveforms, continued

Program Operation



12. TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

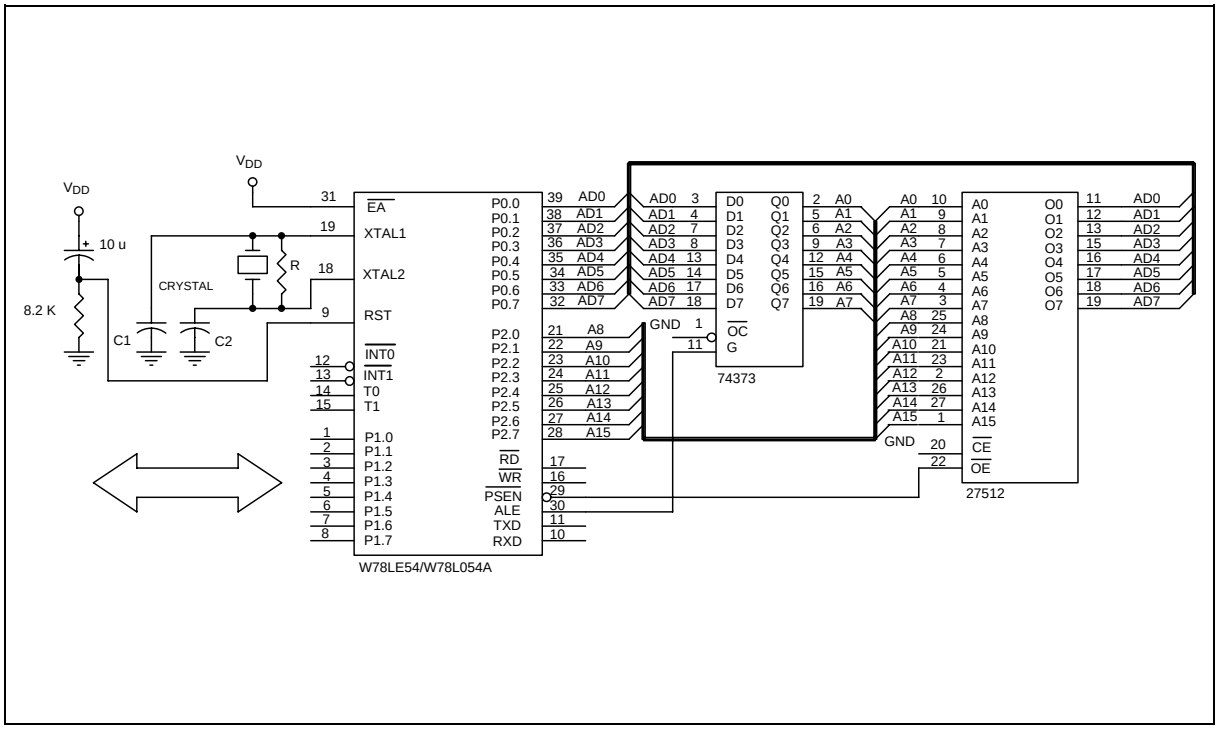


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
20 MHz	15P	15P	-

Above table shows the reference values for crystal applications (full gain).

Note: C1, C2, R components refer to Figure A.

Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

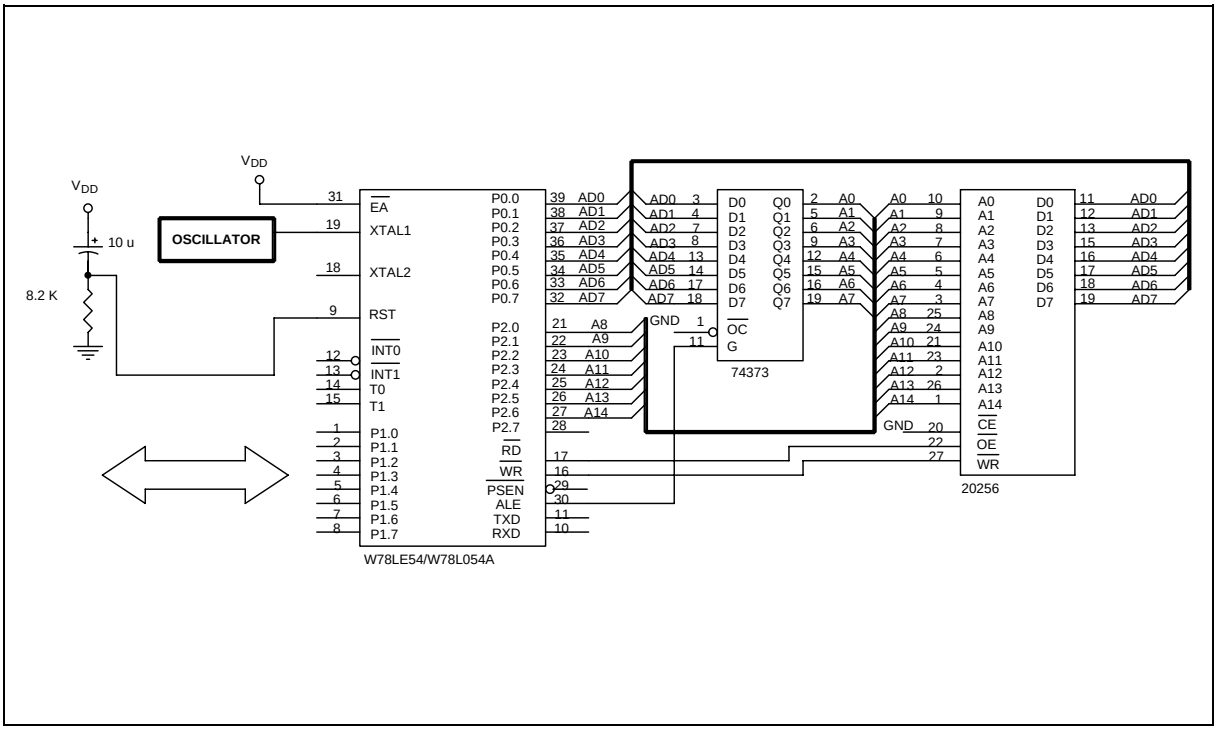
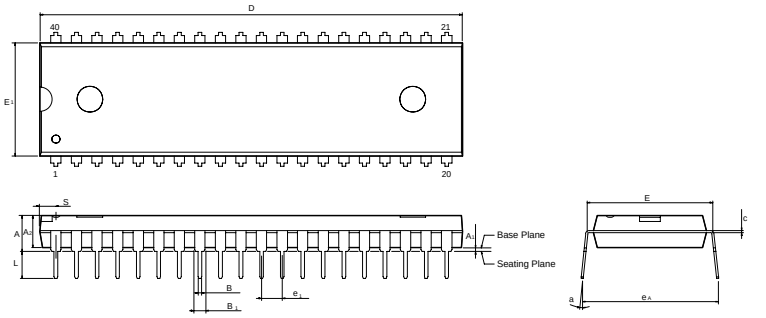


Figure B

13. PACKAGE DIMENSIONS

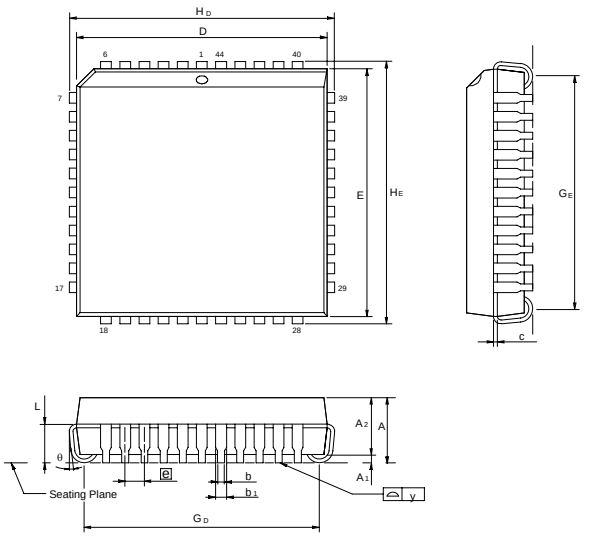
40-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A_1	0.010	—	—	0.254	—	—
A_2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

44-pin PLCC

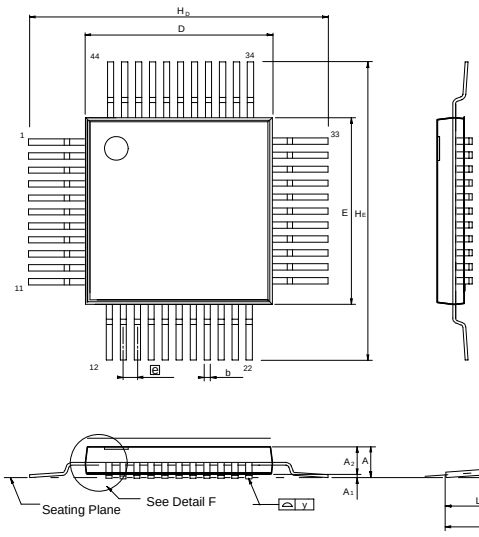


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

REVISION HISTORY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A3	December 2000		-
A4	April 19, 2005	23	Add Important Notice
A5	October 2, 2006		Remove block diagram
A6	December 4, 2006	2	Remove all Leaded package parts

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